

What is Claimed is:

1 1. In a target processor, apparatus for storing a
2 events related to the generation of a trigger signal, the
3 apparatus comprising:

4 a plurality of event signal generation units, each
5 event signal generation unit providing an event signal in
6 response to a preestablished target processor condition

7 a trigger generation unit coupled to the plurality of
8 event signal generation units, the trigger generation unit
9 responsive to at least one preselected event signal for
10 generating an associated trigger signal, the trigger
11 generating unit generating a trigger control signal; and

12 a register, the register having the event signals
13 applied to the trigger unit applied thereto, the register
14 responsive to a trigger control signal generated along with
15 the trigger signal, the trigger control signal causing the
16 register to store event signals applied thereto.

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18 2. The apparatus as recited in claim 1 further
19 comprising at least one event signal generating unit, each
20 event signal generating unit generating an event signal
21 upon identification of a predetermined condition in the
22 target processor.

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24 3. The apparatus as recited in claim 1 further
25 comprising a read bus, wherein a second control signal

1 causes the contents of the register to be applied to the
2 read bus.

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4 4. The apparatus as recited in claim 3 wherein the
5 register is a memory-mapped register.

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7 5. The apparatus as recited in claim 1 further
8 comprising:

9 a second register, the second register
10 responsive to the control signal for storing a program
11 counter address related to the conditions in the target
12 processor resulting in the events signals.

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14 6. The method of storing an events signals resulting
15 in the generation of a trigger signal, the method
16 comprising:

17 generating an event signal for each predetermined
18 event;

19 applying each event signal to a trigger
20 generation unit;

21 applying each event signal to a preselected
22 storage unit location;

23 when a predetermined event signal or
24 predetermined combination of event signals is applied to
25 the trigger generation unit, the trigger generation unit
26 providing a trigger signal and a trigger control signal;
27 and

1 applying the trigger control signal to the
2 storage unit, the storage unit storing the event signals in
3 the storage unit in response to the trigger control signal.

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5 7. The method as recited in claim 6 wherein the
6 storage unit is a register.

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8 8. The method as recited in claim 6 wherein applying
9 a control signal to the storage unit results in application
10 of the contents of the storage unit to a read bus.

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12 9. The method as recited in claim 6 further
13 comprising the step storing program counter address in a
14 second storage unit in response to the trigger control
15 signal.

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17 10. A target processor comprising:
18 at least one event detection unit, each event
19 detection unit responsive to predetermined condition of the
20 target processing unit for generating a related event
21 signal;

22 a trigger generation unit, the trigger generation
23 unit generating trigger signal in response to at least one
24 of the related event signals, the trigger unit generating a
25 trigger control signal when the a trigger signal is
26 generated; and

27 a storage unit, the storage unit coupled to the
28 event detection unit, the storage unit storing each event

1 signal is a related storage unit location in response to
2 the trigger control signal.

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4 11. The target processor as recited in claim 10
5 further comprising a read bus coupled to the storage unit,
6 the event signals stored in the storage unit being applied
7 to the read bus in response to a second control signal.

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9 12. The target processor as recited in claim 11
10 wherein the storage unit is a memory-mapped register
11 accessible to an external test and debug device.

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13 13. The target processor as recited in claim 10
14 further comprising a second storage unit, the second
15 storage unit having a program counter address applied
16 thereto, the storage unit storing applied program counter
17 address in response to the trigger control signal.

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19 14. The target processor as recited in claim 13
20 further comprising a delay line, the delay line delaying
21 the application of the program counter address to the
22 second storage unit for a predetermined period of time.

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24 15. The target processor as recited in claim 14
25 wherein the second storage unit is a memory-mapped
26 register.